METHOD, APPARATUS AND PROGRAM STORAGE DEVICE FOR PROVIDING SELF-QUIESCED LOGIC TO HANDLE AN ERROR RECOVERY INSTRUCTION

ABSTRACT

A method, apparatus and program storage device for providing self-quiesced logic for handling an error recovery instruction such as a reset or self-test instruction. For example, during a reset or self test procedure, the logic is isolated without adversely affecting the local processor. Self-quiesced logic processes an error recovery instruction by monitoring the processor interface for an idle condition and withholding access to the local processor. Once the local processor interface has been quiesced and the internal logic paths are idle, the logic will proceed with the reset or self-test.